a first dopant implant in the capacitor and bit line contact regions, the first dopant having a second conductivity type opposite the first conductivity type, and the first dopant implanted at a dosage of about 10^{13} ions per square centimeter at an implantation energy in the range of 20 KeV to 100 KeV;

insulating spacers extending along the sidewalls of the gate electrode and over a portion of the first dopant implant in the capacitor and bit line contact regions;

a second dopant implant in only the capacitor contact, the second dopant implant having the second conductivity type, and the second dopant implanted at a dosage of about 10^{13} ions per square centimeter at an implantation energy up to 200 KeV;

a capacitor first conductor in electrical contact with the capacitor contact region, the capacitor first conductor comprising polysilicon doped to the second conductivity type to a level in the range of 1×10^{19} to 1×10^{20} atoms per cubic centimeter;

a dielectric over the capacitor first conductor; and

a capacitor second conductor over the dielectric.

REMARKS

Claims 23-28 and 30-33 are pending.

Rejections Under 35 U.S.C. § 102

Claims 23-24 and 26-32 were rejected under 35 U.S.C. § 102(b) as being anticipated by Katayama (U.S. Patent No. 5,444,278).

Katayama does not teach the required second dopant implant into the contact region. Katayama teaches "an n+ diffusion layer 4 formed by thermal diffusion of the impurities (phosphorous) in capacitor lower electrode 9 ...." A diffusion layer is not an implant, and the Examiner makes no specific assertion to the contrary.[1] For this reason alone, Katayama does not anticipate Claims 23-24, 26-28 and 30-32. (Claim 29 has been canceled.)

Katayama also does not teach the further limitations in amended Claims 26 and 27. Claims 26 and 27, as amended, recited that the second dopant implant is

aligned with the insulating spacer extending over the capacitor contact region such that substantially all of the second dopant implant is formed in only that portion of the capacitor contact region not covered by the insulating spacer. This configuration can be seen in Figs. 3-8 and 11-14. Diffusion layer 4 in Katayama is not aligned to the sidewall spacer, but rather extends under the spacer. E.g., Katayama Figs. 1 and 10. For this additional reason, Claims 26 and 27 distinguish patentably over Katayama.

Further with regard to Claim 28, Katayama does not teach a second dopant implanted at an implantation energy up to 200KeV. As noted, diffusion layer 4 in Katayama is formed by diffusion, not implantation. Hence, Katayama cannot and does not teach an implantation energy for diffusion layer 4.

Rejections Under 35 U.S.C. § 103

Claims 25 and 33 were rejected under Section 103 as being obvious over Katayama.

The Section 103 rejection of dependent Claims 25 and 33 is based on the assertion that Katayama teaches all of the limitations of the base claims. For the reasons noted above, this assertion is not correct and Claims 25 and 33 distinguish over Katayama due to their dependence on Claims 23 and 30, respectively.

Also, Katayama does not suggest the further limitations of Claims 25 and 33. Claims 25 and 33 require the depth of the first implant in the range of 500-1000 angstroms and the depth of the second implant is deeper than the first implant up to 2,000 angstroms. Katayama does not say anything about the depth of the first implant and, of course, it doesn't have a second implant and so Katayama can suggest nothing about the depth of any such second implant. It may be true, as the Examiner suggests, that there is a relationship between dosage, energy level and the depth of an implant. Even assuming the Examiner's statement supports Katayama suggesting the depth of the first implant, it is not particularly relevant to the claimed second implant. Katayama doesn't teach a second implant. The diffusion temperature and impurity concentration of the source polysilicon for

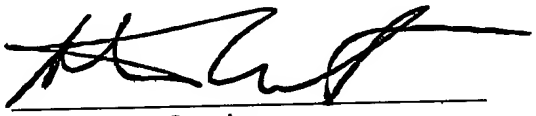
[1] The Examiner characterizes Katayama's diffusion layer 4 as a second dopant "concentration." Office Action, page 2, paragraph 2.

diffusion layer 4 in Katayama suggests nothing about an implant in general, and specifically it says nothing about the depth of the claimed second implant.

For this additional reason, Claims 25 and 33 distinguish over Katayama.

The foregoing is believed to be a complete response to the outstanding Office Action.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES

26.(amended once) A semiconductor memory device, comprising:

a silicon structure having a first conductivity type;

a gate electrode over the silicon structure;

a capacitor contact region in the silicon structure adjacent to one side of the gate electrode;

a bit line contact region in the silicon structure adjacent to the other side of the gate electrode;

a first dopant implant in the capacitor and bit line contact regions, the first dopant having a second conductivity type opposite the first conductivity type;

insulating spacers extending [vertically] along the sidewalls of the gate electrode and [horizontally] over a portion of the first dopant implant in the capacitor and bit line contact regions; and

a second dopant implant in only the capacitor contact region, the second dopant implant aligned with the insulating spacer extending over the capacitor contact region such that substantially all of the second dopant implant is formed in only that portion of the capacitor contact region not covered by the insulating spacer.

27.(amended once) A semiconductor memory device, comprising:

a silicon structure having a first conductivity type;

a gate electrode over the silicon structure having a first conductivity type;

a capacitor contact region in the silicon structure adjacent to one side of the gate electrode;

a bit line contact region in the silicon structure adjacent to the other side of the gate electrode;

a first dopant implant in the capacitor and bit line contact regions, the first dopant having a second conductivity type opposite the first conductivity type;

insulating spacers extending [vertically] along the sidewalls of the gate electrode and [horizontally] over a portion of the first dopant implant in the capacitor and bit line contact regions;

a second dopant implant in only the capacitor contact region, the second dopant implant aligned with the insulating spacer extending over the capacitor contact region such that substantially all of the second dopant implant is formed in only that portion of the capacitor contact region not covered by the insulating spacer;

a capacitor first conductor in electrical contact with the capacitor contact region;

a dielectric over the capacitor first conductor; and

a capacitor second conductor over the dielectric.

28.(amended once) A semiconductor memory device, comprising:

a silicon structure having a first conductivity type;

a gate electrode over the silicon structure;

a capacitor contact region in the silicon structure adjacent to one side of the gate electrode;

a bit line contact region in the silicon structure adjacent to the other side of the gate electrode;

a first dopant implant in the capacitor and bit line contact regions, the first dopant having a second conductivity type opposite the first conductivity type, and the first dopant implanted at a dosage of about 10^{13} ions per square centimeter at an implantation energy in the range of 20 KeV to 100 KeV;

insulating spacers extending [vertically] along the sidewalls of the gate electrode and [horizontally] over a portion of the first dopant implant in the capacitor and bit line contact regions;

a second dopant implant in only the capacitor contact, the second dopant implant having the second conductivity type, and the second dopant implanted at a dosage of about 10^{13} ions per square centimeter at an implantation energy up to 200 KeV;

a capacitor first conductor in electrical contact with the capacitor contact region, the capacitor first conductor comprising polysilicon doped to the second conductivity type to a level in the range of 1×10^{19} to 1×10^{20} atoms per cubic centimeter;

a dielectric over the capacitor first conductor; and

a capacitor second conductor over the dielectric.